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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/859,659	05/17/2001	John K. Walton	EMC2-090PUS	3903

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	8

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/859,659	Applicant(s) WALTON, JOHN K.	
	Examiner Guy J. Lamarre, P.E.	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

0. This office action is in response to Applicants' **Amendment** of *9 Feb. 2004.*

0.1 **Claims 1, 3, 5, 7, 9-14** are amended. **Claims 1-14** remain pending.

0.2 The prior art rejections and objections of record are withdrawn in response to Applicants' **Amendment.**

Response to Arguments

1. Applicants' arguments of *9 Feb. 2004* have been fully considered: they are found persuasive only to the extent that the feature whereby NOOP cammand is invoked on finding dissimilar address/control portions after checking operations which is equivalent to a feature whereby data transfer is inhibitted subsequent to error detection is not specifically described by the prior art of record. However, Bock et al. (US Patent No. 5,948,119) teaches such feature in e.g., Fig. 13.

Claim Rejections - 35 USC ' 103

2. Claim(s) 1-14 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Richter U.S. Patent No. 4,245,344 (hereinafter Richter) in view of Cloonan U.S. Patent No. 5,566,193 (hereinafter Cloonan) in further view of **Bock et al.** (US Patent No. 5,948,119; 7 Sept. 1997).

As per claims 1-14,

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory and related coupling means, see column 5, lines 5-20. The parity checkers 127 and 128 of Figure 4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the two parity checkers 127 and

128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches of a write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the received signals or their parity checks are not equal), the control (or the checker) insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections. Nonetheless, Richter does teach of preventing the use of erroneous signals by comparing the parity of the two signals and of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Cloonan to provide serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract,

lines 1-3. Also, both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

Richter teaches of preventing the writing of data to memory when an error is detected, see column 6, lines 25-35. Further, Richter teaches of insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27. While Richter does not explicitly teach of the NOOP command causing the storage to be inhibited, Richter does suggest that when an error is detected, an instruction causes the storage to be inhibited. Further, a NOOP command is a command in which the instruction is to do nothing. In other words a NOOP command simply tells the device receiving the instruction to do nothing. The claimed limitations, however, read that a NOOP instruction is used to produce a certain action/desired output. Therefore the Examiner is viewing the NOOP instruction simply as an instruction causing the memory/data to not be written to memory. Once read in this light, it is clear that Richter teaches of a issuing an instruction to inhibit the writing to memory of data once the data is found to have an error.

Examiner **also notes that** the approach of inhibiting data transfer when a system failure or error is detected based on error detection means is disclosed by e.g. **Bock et al.,** in Abstract and Fig. 13: block 230 and associated description in col. 1 line 55 et seq., hardware and an algorithm for dynamically inhibiting data transfer when a system failure or error is detected based on CRC or other error detection means wherein such techniques are described based on error detection including means to inhibit data transfer by comparing CRC values (col. 1 line 65) and taking appropriate corrective steps, such as transferring such erroneous data to an output device for further processing subsequent to delaying such data to allow for such detection to complete (col. 2 line 1). Inhibiting transfer of such erroneous data may also be effected via summarily discarding such erroneous data via a selecting arrangement the implementation of

which is stark clear to those of ordinary skill in the art (col. 2 line 3). Such selecting arrangement is configured to transfer time-delayed data to a 1st destination or to plural other destinations based on CRC status. {See **Bock et al.,** Id., Figs. 1-22 and associated description in, e.g., col. 1 line 15 et seq., including means to fragment original data into plural sub-blocks with CRC appended thereto in Fig. 5, and sub-block clocking means in Fig. 7: block 152. For Example, at col. 19 line 18 et seq., "Referring to FIG. 13, a portion 230 of the packet FIFO unit 178 includes hardware for handling receipt of data packets. The hardware handles validation and storage of each packet received. If a **received packet is deemed invalid** because the calculated CRC does not match the translated CRC, **then the entire packet is discarded** and none of the data therein is provided to any other portion of the receiver. Packets of data are either discarded or retained in their entirety." **In other words, data storage** or NOOP command means **is inhibited when such data is erroneous or on some predetermined condition**.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the data transfer of Richter and Cloonan by including therein data transmission or storage prevention means based on error or CRC status or NOOP command means, as taught by **Bock et al.,** because such modification would provide the procedure disclosed in Richter and Cloonan with a technique whereby "only error-free *data transfer is allowed, such transfer being dynamically based on the quality of the transmission line or channel so as to improve data processing and reduce communications system energy consumption since unnecessary data transfer is eliminated.*" {See **Bock et al., Id.,** col. 2 line 1 et seq.}

As per claim 2,

Both of the above cited references substantially teach, as combined above in claim 1, the limitations of claim 2.

With respect to the limitations of claim 2, Richter teaches of preventing the writing of data to memory when an error is detected, see column 6, lines 25-35. Further, Richter teaches of insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27. While Richter does not explicitly teach of the NOOP command causing the storage to be inhibited, Richter does suggest that when an error is detected, an instruction causes the storage to be inhibited. Further, a NOOP command is a command in which the instruction is to do nothing. In other words a NOOP command simply tells the device receiving the instruction to do nothing. The claimed limitations, however, read that a NOOP instruction is used to produce a certain action/desired output. Therefore the Examiner is viewing the NOOP instruction simply as an instruction causing the memory/data to not be written to memory. Once read in this light, it is clear that Richter teaches of a issuing an instruction to inhibit the writing to memory of data once the data is found to have an error.

Examiner **also notes that** the approach of inhibiting data transfer when a system failure or error is detected based on error detection means is disclosed by e.g. **Bock et al.,** in Abstract and Fig. 13: block 230 and associated description in col. 1 line 55 et seq., hardware and an algorithm for dynamically inhibiting data transfer when a system failure or error is detected based on CRC or other error detection means wherein such techniques are described based on error detection including means to inhibit data transfer by comparing CRC values (col. 1 line 65) and taking appropriate corrective steps, such as transferring such erroneous data to an output device for further processing subsequent to delaying such data to allow for such detection to complete (col. 2 line 1). Inhibiting transfer of such erroneous data may also be effected via summarily discarding such erroneous data via a selecting arrangement the implementation of which is stark clear to those of ordinary skill in the art (col. 2 line 3). Such selecting arrangement

is configured to transfer time-delayed data to a 1st destination or to plural other destinations based on CRC status. {See **Bock et al.,** Id., Figs. 1-22 and associated description in, e.g., col. 1 line 15 et seq., including means to fragment original data into plural sub-blocks with CRC appended thereto in Fig. 5, and sub-block clocking means in Fig. 7: block 152. For Example, "Referring to FIG. 13, a portion 230 of the packet FIFO unit 178 includes hardware for handling receipt of data packets. The hardware handles validation and storage of each packet received. If a **received packet is deemed invalid** because the calculated CRC does not match the translated CRC, **then the entire packet is discarded** and none of the data therein is provided to any other portion of the receiver. Packets of data are either discarded or retained in their entirety." **In other words, data storage** or NOOP command means **is inhibited when such data is erroneous or on some predetermined condition**.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the data transfer of Richter and Cloonan by including therein data transmission or storage prevention means based on error or CRC status or NOOP command means, as taught by **Bock et al.,** because such modification would provide the procedure disclosed in Richter and Cloonan with a technique whereby "only error-free *data transfer is allowed, such transfer being dynamically based on the quality of the transmission line or channel so as to improve data processing and reduce communications system energy consumption since unnecessary data transfer is eliminated.*" {See **Bock et al., Id.,** col. 2 line 1 et seq.}

As per claim 3,

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory, see column 5, lines

5-20. The parity checkers 127 and 128 of Figure 4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the two parity checkers 127 and 128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches or write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the parity checks aren't equal), the control (or the checker) ensuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections or specifically of the parity of the address/control portion being used. Nonetheless, Richter does teach of preventing the use of erroneous signals by comparing the parity of the two signals and of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been

motivated by the suggestion provided by Cloonan to provide serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract, lines 1-3. Both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

Further, it would have been obvious to one of ordinary skill in the art to use the parity of a specific part of received data to determine if two received packets are without error. Specifically, it is not uncommon for two packets of data to have the same payload with different destinations. In this case, it would be obvious to one of ordinary skill to want to use the parity of the address section only to determine the validity of received packets.

As per claim 4,

Both of the above cited references substantially teach, as combined above in claim 3, the limitations of claim 4.

With respect to the limitations of claim 2, Richter teaches of preventing the writing of data to memory when an error is detected, see column 6, lines 25-35. Further, Richter teaches of insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27. While Richter does not explicitly teach of the NOOP command causing the storage to be inhibited, Richter does suggest that when an error is detected, an instruction causes the storage to be inhibited. Further, a NOOP command is a command in which the instruction is to do nothing. In other words a NOOP command simply tells the device receiving the instruction to do nothing. The claimed limitations, however, read that a NOOP instruction is used to produce a certain action/desired output. Therefore the Examiner is viewing the NOOP instruction simply as an instruction causing the memory/data to not be written to memory. Once read in this light, it is clear that Richter teaches of a issuing an instruction to inhibit the writing to memory of data once

the data is found to have an error. Also see **Bock et al.,** Id., at col. 19 line 18 et seq., "Referring to FIG. 13, a portion 230 of the packet FIFO unit 178 includes hardware for handling receipt of data packets. The hardware handles validation and storage of each packet received. If a **received packet is deemed invalid** because the calculated CRC does not match the translated CRC, **then the entire packet is discarded** and none of the data therein is provided to any other portion of the receiver. Packets of data are either discarded or retained in their entirety." **In other words, data storage** or NOOP command means **is inhibited when such data is erroneous or on some predetermined condition**.

As per claim 5,

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory, see column 5, lines 5-20. The parity checkers 127 and 128 of Figure 4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the two parity checkers 127 and 128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches or write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the parity checks aren't equal), the control (or the checker) ensuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections or specifically of the parity of the entire digital word being used. Nonetheless, Richter does teach

of preventing the use of erroneous signals by comparing the parity of the two signals and of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Cloonan to provide serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract, lines 1-3. Both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

Further, it would have been obvious to one of ordinary skill in the art to use the parity of the entire digital word to determine if two received packets are without error. As noted above, it is not uncommon for two packets to contain the same data for different addresses. One method, as noted in claim 5 is to only compare the address portion. Along the same lines, one skilled in the art could just as easily implement the parity check to check the entire word (i.e. address and data portions). One skilled in the art would want to do this so as to offer better protection from erroneously comparing two unrelated words destined for the same address. By comparing the

entire word (address and data) one skilled in the art can be more certain of the validity/invalidity of the received data.

As per claim 6,

Both of the above cited references substantially teach, as combined above in claim 5, the limitations of claim 6.

With respect to the limitations of claim 6, Richter teaches of preventing the writing of data to memory when an error is detected, see column 6, lines 25-35. Further, Richter teaches of insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27. While Richter does not explicitly teach of the NOOP command causing the storage to be inhibited, Richter does suggest that when an error is detected, an instruction causes the storage to be inhibited. Further, a NOOP command is a command in which the instruction is to do nothing. In other words a NOOP command simply tells the device receiving the instruction to do nothing. The claimed limitations, however, read that a NOOP instruction is used to produce a certain action/desired output. Therefore the Examiner is viewing the NOOP instruction simply as an instruction causing the memory/data to not be written to memory. Once read in this light, it is clear that Richter teaches of a issuing an instruction to inhibit the writing to memory of data once the data is found to have an error. Also see **Bock et al.,** Id., at col. 19 line 18 et seq., "Referring to FIG. 13, a portion 230 of the packet FIFO unit 178 includes hardware for handling receipt of data packets. The hardware handles validation and storage of each packet received. If a **received packet is deemed invalid** because the calculated CRC does not match the translated CRC, **then the entire packet is discarded** and none of the data therein is provided to any other portion of the receiver. Packets of data are either discarded or retained in their entirety." **In other words, data storage** or NOOP command means **is inhibited when such data is erroneous or on some predetermined condition**.

As per claim 7,

Both of the above cited references substantially teach, as combined specifically above in claims 3 and 5, the limitations of claim 7.

With respect to the limitations of claim 7, the limitations are identical to the limitations set forth in claims 3 and 5 with the exception that the causes of a NOOP instruction are combined.

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory, see column 5, lines 5-20. The parity checkers 127 and 128 of Figure 4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the two parity checkers 127 and 128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches or write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the parity checks aren't equal), the control (or the checker) ensuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections or specifically of the parity of the address/control portion being used. Nonetheless, Richter does teach of preventing the use of erroneous signals by comparing the parity of the two signals and

of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Cloonan to provide serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract, lines 1-3. Both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

Further, it would have been obvious to one of ordinary skill in the art to use the parity of a specific part of received data to determine if two received packets are without error. Specifically, it is not uncommon for two packets of data to have the same payload with different destinations. In this case, it would be obvious to one of ordinary skill to want to use the parity of the address section only to determine the validity of received packets. Further, it would have been obvious to one of ordinary skill in the art to also use the parity of the entire digital word to determine if two received packets are without error. As noted above, it is not uncommon for two packets to contain the same data for different addresses. One skilled in the art could just as easily implement the parity check to check the entire word (i.e. address and data portions). One

skilled in the art would want to do this so as to offer better protection from erroneously comparing two unrelated words destined for the same address. By comparing the entire word (address and data) one skilled in the art can be more certain of the validity/invalidity of the received data. In view of both of the above methods, it is clear that one is geared toward speed (checking the parity of the address/control takes less time than the entire word) and the other geared towards higher reliability (checking the parity of the entire digital word ensures that the correct/incorrect word is detected). One of ordinary skill would want to have both types of detection because the address/control checking disposes of errors quickly and the entire word checking is more exact in the detection of errors.

As per claim 8,

Both of the above cited references substantially teach, as combined above in claim 7, the limitations of claim 8.

With respect to the limitations of claim 8, Richter teaches of preventing the writing of data to memory when an error is detected, see column 6, lines 25-35. Further, Richter teaches of insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27. While Richter does not explicitly teach of the NOOP command causing the storage to be inhibited, Richter does suggest that when an error is detected, an instruction causes the storage to be inhibited. Further, a NOOP command is a command in which the instruction is to do nothing. In other words a NOOP command simply tells the device receiving the instruction to do nothing. The claimed limitations, however, read that a NOOP instruction is used to produce a certain action/desired output. Therefore the Examiner is viewing the NOOP instruction simply as an instruction causing the memory/data to not be written to memory. Once read in this light, it is clear that Richter teaches of a issuing an instruction to inhibit the writing to memory of data once

the data is found to have an error. Also see **Bock et al.,** Id., at col. 19 line 18 et seq., "Referring to FIG. 13, a portion 230 of the packet FIFO unit 178 includes hardware for handling receipt of data packets. The hardware handles validation and storage of each packet received. If a **received packet is deemed invalid** because the calculated CRC does not match the translated CRC, **then the entire packet is discarded** and none of the data therein is provided to any other portion of the receiver. Packets of data are either discarded or retained in their entirety." **In other words, data storage** or NOOP command means **is inhibited when such data is erroneous or on some predetermined condition**.

As per claim 9,

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory, see column 5, lines 5-20. The parity checkers 127 and 128 of Figure 4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the two parity checkers 127 and 128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches of a write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the received signals or their parity checks are not equal), the control (or the checker) insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections or of a checker comprising a parity generator. Nonetheless, Richter does teach of preventing the use of

erroneous signals by comparing the parity of the two signals and of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Cloonan to provide serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract, lines 1-3. Also, both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

Further, Richter teaches that depending on the inputs to the control, 120 of Figure 4, the write enable line, 164 will either be allowed or inhibited. Richter teaches of the equations that are used to determine whether a failure has occurred, see column 5, lines 55-65. These equations determine whether or not an input error has occurred and therefore perform equivalent to the parity generator of the checker. One skilled in the art would see that the inputs cause the write enable (as a digital signal) as a 0 or 1 value with, i.e., 1 being allowed and 0 being inhibited. Still further, if the write enable is inhibited, there had to have been some kind of input error. As noted above, an error will inhibit write enable, in essence causing a 0, or inverted signal/bit, to be outputted. Similarly, if there are no errors present, a 1 will be outputted.

Still further, one skilled in the art could use the parity bit comparisons to determine if the packets are the same or different (see control unit 120 of Figure 4), or if the entire digital words are the same or different (see compare 125 of Figure 4).

As per claim 10,

All of the above cited references substantially as combined above in claim 9, the claimed limitations of claim 10.

With respect to the limitations of claim 10, it would have been obvious to one of ordinary skill in the art to send an inverted bit (i.e. 0 or inhibit the write enable) if the parity bits disagree or if the digital words disagree, both of which are indications that there has been an error in the input. Also see **Bock et al.,** Id., at col. 19 line 18 et seq., "Referring to FIG. 13, a portion 230 of the packet FIFO unit 178 includes hardware for handling receipt of data packets. The hardware handles validation and storage of each packet received. If a **received packet is deemed invalid** because the calculated CRC does not match the translated CRC, **then the entire packet is discarded** and none of the data therein is provided to any other portion of the receiver. Packets of data are either discarded or retained in their entirety." **In other words, data storage** or NOOP command means **is inhibited when such data is erroneous or on some predetermined condition**.

As per claim 11,

All of the above cited references substantially teach, as combined above in claim 9, the claimed limitations of claim 11.

With respect to the limitations of claim 11, Richter further teaches of a data port for receiving the data and the address/control information, see Figure 3 where the data packet has address and data information. Still further, Richter, in Figure 4 teaches of an address/control port connected to the memory, see Address IN port, on memory element 166 of Figure 4, and of a write port, see Data In of Figure 4.

As per claim 12,

All of the above cited references substantially teach, as combined above in claim 9, the claimed limitations of claim 12.

With respect to the limitations of claim 12, it would have been obvious to one of ordinary skill in the art to send an inverted bit (i.e. 0 or inhibit the write enable) if the parity bits disagree or if the digital words disagree, both of which are indications that there has been an error in the input.

As per claim 13,

All of the above cited references substantially teach, as combined above in claim 9, the claimed limitations of claim 13.

With respect to the limitations of claim 13, Richter teaches of a communication system between processors and memory, see column 1, lines 1-10 and of two way communication, see column 3, lines 1-5. Richter further teaches of an input port see the inputs to control 120 of Figure 4, for transmitting data from memory and of a read data port, see data out port of memory elements 166 of Figure 4, for reading data out of memory.

Further, Richter teaches that depending on the inputs to the control (checker), 120 of Figure 4, the write enable line, 164 of Figure 4, will either be allowed or inhibited. Richter teaches of the equations that are used to determine whether a failure has occurred, see column 5, lines 55-65. These equations determine whether or not an input error has occurred and therefore perform equivalent to the parity generator of the checker. One skilled in the art would see that the inputs cause the write enable (as a digital signal) as a 0 or 1 value with, i.e., 1 being allowed and 0 being inhibited. Still further, if the write enable is inhibited, there had to have been some kind of input error. As noted above, an error will inhibit write enable, in essence causing a 0, or inverted signal/bit, to be outputted. Similarly, if there are no errors present, a 1 will be outputted.

While not explicitly disclosing an inverter, Richter does teach of allowing or inhibiting the write enable line. Since one signal will be high and one will be low, it is clear that an inverter, or equivalent, can be used to do so.

Still further, one skilled in the art could use the parity bit comparisons to determine if the packets are the same or different (see control unit 120 of Figure 4), or if the entire digital words are the same or different (see compare 125 of Figure 4). Further, it would have been obvious to one of ordinary skill in the art to use a selector, or equivalent, to choose between sending an inverted (i.e. 0 and hence inhibiting) signal or a enable (i.e. 1) signal out if the parity bits or digital words were the same (enable) or different (inhibit).

As per claim 14,

All of the above cited references substantially teach, as combined above in claim 9, the claimed limitations of claim 14.

With respect to the limitations of claim 14, it would have been obvious to one of ordinary skill in the art to send an inverted bit (i.e. 0 or inhibit the write enable) if the parity bits disagree or if the digital words disagree, both of which are indications that there has been an error in the input.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

3.1 Any response to this action should be mailed to:

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached on (703) 305-9595.

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Guy J. Lamarre, P.E
Primary Examiner
4/25/04